Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-14. (cancelled)

15. (currently amended) A composite layer of low k silicon oxide dielectric material on an oxide layer of an integrated circuit structure, said composite layer of low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions between metal lines, deposition rates in other regions comparable to standard k silicon oxide, and without exhibiting via poisoning characteristics, comprising:

a) a first layer of low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions, deposited until said first layer of low k silicon oxide dielectric material completely fills said high aspect ratio regions between said metal lines and reaches the level of the top of metal lines on said oxide layer; and

b) a second layer of low k silicon oxide dielectric material deposited over said [[the]] first layer of low k silicon oxide dielectric material at a faster rate than the deposition rate of said first layer up to the desired overall thickness of the composite layer of low k ~~carbon doped~~ silicon oxide dielectric material.

16. (original) The composite layer of low k silicon oxide dielectric material of claim 15 wherein said first and second layers comprising said composite layer of low k silicon oxide dielectric material are all formed in a single vacuum processing apparatus without removal of said semiconductor substrate from said vacuum apparatus.

17. (original) A composite layer of low k carbon-doped silicon oxide dielectric material on an oxide layer of an integrated circuit structure on a semiconductor substrate, said composite layer of low k carbon-doped silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions, deposition rates comparable to non carbon-doped silicon oxide, and without exhibiting via poisoning characteristics, comprising:

a) a first layer of low k carbon-doped silicon oxide dielectric material formed by reacting a carbon-substituted silane reactant with hydrogen peroxide until the resulting deposition of low k carbon-doped silicon oxide dielectric material reaction product reaches the level of the top of metal lines on the oxide layer; and

b) a second layer of carbon-doped low k silicon oxide dielectric material formed over said first layer by plasma enhanced chemical vapor deposition (PECVD) up to the desired overall thickness of the low k carbon-doped silicon oxide dielectric layer.

18. (currently amended) A composite layer of low k silicon oxide dielectric material on an oxide layer of an integrated circuit structure on a semiconductor substrate having closely spaced apart metal lines thereon, said composite layer of low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions between closely spaced apart metal lines, deposition rates in other regions comparable to standard k silicon oxide, and without exhibiting via poisoning characteristics, and said composite layer further comprising:

a) a first layer of low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions between said closely spaced apart metal lines, said first layer of low k silicon oxide dielectric material formed over said oxide layer and said metal lines up to at least the level of the top of said metal lines on said oxide layer, to completely fill said high aspect ratio regions between said metal lines, and planarized down to said top of said metal lines; and

b) a second layer of low k silicon oxide dielectric material over said planarized first layer and said top of said metal lines, said second layer of low k silicon oxide dielectric material deposited at a higher deposition rate than said first low k layer.

19. (previously presented) A composite layer of low k carbon-doped silicon oxide dielectric material on an oxide layer of an integrated circuit structure on a semiconductor substrate, said composite layer of low k carbon-doped silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions between closely spaced apart metal lines, deposition rates comparable to non carbon-doped silicon oxide, and without exhibiting via poisoning characteristics, said composite layer further comprising:

a) a first layer of low k carbon-doped silicon oxide dielectric material formed over said oxide layer and said metal lines by reacting a carbon-substituted silane reactant with hydrogen peroxide until the resulting deposition of low k carbon-doped silicon oxide dielectric material reaction product reaches at least the level of the top of said metal lines on the oxide layer to form a low k silicon oxide dielectric material exhibiting void-free deposition properties in high aspect ratio regions between said closely spaced apart metal lines, said first layer of low k silicon oxide dielectric. material planarized down to said top of said metal lines; and

b) a second layer of carbon-doped low k silicon oxide dielectric material formed over said planarized first layer and over said tops of said metal lines up to the desired overall thickness of the low k carbon-doped silicon oxide dielectric layer by plasma enhanced chemical vapor deposition (PECVD), said second layer of low k silicon oxide dielectric material deposited at a higher deposition rate than said first layer.